

Substitute for form 1449A-PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Application Number

Filing Date

First Named Inventor

Art Unit

Examiner Name

Attorney Docket Number

PTO/SB/08A

10/31/2002. OMB 06

DEPARTMENT OF COMMERCE

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COOKE, et al.

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262 Thompson

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YY	Name of Patentee or Application of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
	1	US-5,553,002	09/1996	DANGELO, et al.	

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		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
	2	WO 95/31778 PCT	11/23/1995			
	3	WO 97/46959 PCT	12/11/1997			
	4	WO 98/13776 PCT	04/02/1998			

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher city and/or country where published	T ²
	5	ABRAMOVICI, Miron et al., "Digital Systems Testing and Testable Design" <i>IEEE Press Marketing</i> (September 1994).	
	6	ANDERSON, T.L. et al., "Thoughts on Core Integration and Test," <i>Proceedings - International Test Conference</i> (1997), pg. 1039.	
	7	BAUER, M. et al., "Hardware/Software Co-Simulation in a VHDL-based Test Bench Approach," <i>Proceedings of the Design Automation Conference, US, New York, ACM</i> (1997), 34:774-779.	
	8	GLASER, Steve, "IP Fuels A Transformation of Culture, Companies, and Cooperation," <i>Electronic Design</i> , January 12, 1998, pp. 55-62.	
	9	GUPTA, R.K. et al., "Introducing Core-Based System Design," <i>IEEE Design and Test of Computers</i> (1997), 14(4):15-24.	
	10	KEATING, Michael et al., "Reuse Methodology Manual for System-On-A-Chip Designs" <i>Kluwer Academic Publishers</i> (1998).	
	11	PASSERONE, R. et al., "Automatic Synthesis of Interfaces Between Incompatible Protocols," <i>Proceedings 1998 Design and Automation Conference</i> (1998), pp. 8-13.	
	12	REMAKLUS, W., "On-Chip Bus Structure for Custom Core Logic Designs," <i>IEEE</i> (1998), pp. 7-14.	
	13	RINCON, A.M. et al., "Core+ASIC Methodology: The Pursuit of System-on-a-Chip," <i>WESCON/97 Conference Proceedings</i> (1997), PP. 46-54.	
	14	ROWSON, J.A. et al., "Interface-Based Design," <i>Proceedings 1997 Design Automation Conference</i> (1997), pp. 9-13.	
	15	SACHS, H., "All-Inclusive Approach to System Design Offers Flexibility Over Single On-chip Bus Method," <i>Computer Design</i> (1995), 37(7): 97-98.	
	16	SCHÜTZ, M., "How to Efficiently Build VHDL Testbenches," <i>IEEE</i> (1995) 554-559.	
	17	VAN DE GOOR, A.J., "Testing Semiconductor Memories Theory and Practice" <i>Delft University of Technology, The Netherlands, published by John Wiley</i> (1991).	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 2 of 2

Complete if Known

Application Number	09/812,068
Filing Date	March 19, 2001
First Named Inventor	Laurence H. COOKE, et al.
Art Unit	2825
Examiner Name	Annette M. Thompson
Attorney Docket Number	262/043; 19535-7078

18	ZORIAN, Y., "Test Requirements for Embedded Core-based Systems and IEEE P1500," International Test Conference (1997) 28: 191-198.	
19	"Integrated Set of Design Verification Tools," IBM Technical Disclosure Bulletin (1995), 38(5): 329-333.	
20	"The National Technology Roadmap for Semiconductors" (1997). <u>SEMICONDUCTOR INDUSTRY ASSOCIATION</u>	
21	Virtual Socket Interface Alliance Architecture Document, Version 1.0 (March 1997).	
22	Virtual Socket Interface Alliance Analog/Mixed-Signal Development Working Group Specification 1 Version 1.0 (AMS 1 1.0) "Analog/Mixed-Signal VSI Extension" (June 15, 1998).	
23	Virtual Socket Interface Alliance Implementation/Verification Development Working Group Specification 1 Version 1.0 (I/V 1 1.0) "Structural Netlist and Hard VC Physical Data Types" (June 15, 1998)	
24	Virtual Socket Interface Alliance On-Chip Bus Development Working Group Specification 1 Version 1.0 (OCB 1 1.0) "On-Chip Bus Attributes" (August 8, 1998).	

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Sheet 1 of 1

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U.S. Dept. of Commerce
Patent and Trademark Office

Atty Docket No.
21891.01301

Serial No.
09/410,356

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Applicant

Henry Chang et al.

Filing Date

September 30, 1999

Group

2825

U.S. PATENT DOCUMENTS

*Examiner Initials	Document Number	Date	Name	Class	Subclass	Filing Date
AA						
AB						
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AD						
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AG						
AH						

FOREIGN PATENT DOCUMENTS

Document Number	Date	Country	Class	Subclass	Translation
					Yes No
AI					

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	AK	Michael Keating and Pierre Bricaud, "Reuse Methodology Manual for System-On-A-Chip Designs", Kluwer Academic Publishers, 1998. no page numbers
	AL	Virtual Socket Interface Alliance Architecture Document, Version 1.0, March 1997, no page numbers, author
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	AP	"National Technology Roadmap for Semiconductors", 1997, no page numbers, author
	AQ	Steve Glaser, "IP fuels a transformation of culture, companies and cooperation". Electronic Design, January 12, 1998, pp. 55-62.
	AR	"Digital Systems Testing and Testable Design" revised ed. By Miron Abramovici, Melvin A. Breuer, and Arthur Friedman, IEEE Press Marketing, 09/1984, no page numbers
	AS	A J Van de Goor, "Testing Semiconductor Memories: Theory and Practice", Delft Univ. of Technology, The Netherlands, published by John Wiley, 1991, no page numbers

Examiner

WJ Sabili

Date Considered

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